R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns a system generally comprising a formatter, an error correction encoder, an interleave module, an inserter and a turbo encoder. The formatter may be configured to format a plurality of data frames received in a transport stream by inserting a plurality of synchronization data to produce a block stream. The error correction encoder may be configured to encode the block stream to produce an error protected block stream. The interleave module may be configured to interleave the error protected block stream to produce a data stream. The inserter may be configured to insert a synchronization signal into the data stream. The turbo encoder may be configured to encode the data stream to produce an encoded stream.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments can be found in the specification, for example, on page 5 lines 1-8, page 15 lines 9-10 and FIGS. 1 and 12, as originally filed. Thus, no new matter has been added. The claim amendments should only require a cursory review and thus should be entered per MPEP §714.13.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 22 and 24 under 35 U.S.C. §112, first paragraph for failing to comply with the written description requirement is respectfully traversed and should be withdrawn. The claimed limitation of 2 errors per 10,000 bits is disclosed on page 18, line 1 of the specification as originally filed. The claimed limitation of 3 errors per 100,000 bits is disclosed on page 17, line 11 of the specification as originally filed. As such, the claims are compliant with the written description requirement.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-20 under 35 U.S.C. §103(a) as being unpatentable over Citta et al. '889 (hereafter Citta) in view of Yi '427 is respectfully traversed and should be withdrawn.

Citta concerns a trellis coded modulation system for HDTV (Title). Yi concerns a communications system handoff operation combining turbo coding and soft handoff techniques (Title). Citta and Yi, alone or in combination, do not appear to teach or suggest every element in the claims. Furthermore, *prima facie* obviousness to combine the references has not been established for lack of evidence for (i) clear and particular motivation to combine and (ii) a reasonable expectation of success. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

"[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicants."[1] "[T]he factual inquiry whether to combine references must be thorough and searching."[2] "This factual question ... [cannot] be resolved on subjective belief and unknown authority."[3] "It must be based on objective evidence of record."[4] The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations as arranged in the claims.[5] Furthermore, The Court of Appeals for the Federal Circuit has indicated that the requirement

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[1] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

[2] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

[3] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[4] *Id.* at 1343, 61 USPQ2d at 1434.

[5] Manual of Patent Examining Procedure (MPEP), Eighth Edition, Revised February 2003, §2142.

for showing the teaching of motivation to combine references is "rigorous" and must be "clear and particular".[6]

Claim 1 provides a formatter configured to format a plurality of data frames received in a transport stream by inserting a plurality of synchronization data to produce a block stream. Assuming, *arguendo*, that the signal generated by the Data Source 24 of Citta is similar to the claimed block stream (for which Applicants' representative does not necessarily agree), Citta appears to be silent regarding the Data Source 24 operating on a transport stream. Yi does not appear to cure the lack of a transport stream in Citta. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest a formatter configured to format a plurality of data frames received in a transport stream by inserting a plurality of synchronization data to produce a block stream as presently claimed.

Citta also appears to be silent regarding the Data Source 24 inserting a plurality of synchronization data into the data frames of a transport stream. Yi does not appear to cure the missing insertion deficiency of Citta. Page 10, Examiner's Response, line "b" of the Office Action cites a Mapper and Sync Inserter 34 from FIG. 2A of Citta for inserting synchronization data into the data frames of a signal. However, page 3, section 4,

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[6] *In re Anita Dembiczak* and *Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999)

line "e" of the Office Action cites the same Mapper and Sync Inserter 34 of Citta for inserting a synchronization signal into another signal. Since the single Mapper and Sync Inserter 34 of Citta cannot generate and insert both synchronization data and a synchronization signal into two different signals at the same time, the Office Action has failed to establish that Citta and Yi, alone or in combination, teach or suggest at least one of the formatter and the inserter as presently claimed.

Claim 1 further provides an inserter configured to insert a synchronization signal into the data stream and a turbo encoder configured to encode the data stream. Assuming, *arguendo*, that it would have been obvious to modify Citta by replacing the trellis encoder 32 with the Turbo Encoder 502 of Yi (for which Applicants' representative does not necessarily agree), the resulting circuit does not teach or suggest a turbo encoder operating on a stream having a synchronization signal. In particular, the encoder 34 (as modified) appears to operate on a stream without the synchronization signal. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest an inserter configured to insert a synchronization signal into the data stream and a turbo encoder configured to encode the data stream as presently claimed.

Assuming, *arguendo*, that the proposed combination of Citta and Yi includes moving the Mapper and Sync Inserter 34 of

Citta ahead of the encoder 32 (for which the Applicants' representative does not necessarily agree), the Office Action has failed to provide any evidence of (i) motivation to make such a change and (ii) a reasonable expectation of success as required by MPEP §2142. The fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness.[7] Therefore, *prima facie* obviousness has not been established to modify Citta such that the encoder 34 operates on a stream including a synchronization signal inserted by the Mapper and Sync Inserter 34.

Furthermore, the Office Action has cited the Mapper and Sync Inserter 34 of Citta for both the claimed formatter and the claimed inserter. Therefore, the Office Action has failed to establish that Citta and Yi, alone or in combination, teach or suggest at least one of a formatter and an inserter as presently claimed.

Furthermore, the Office Action has not established *prima facie* obviousness for lack of motivation to combine the references. Appendix A paragraph 9.1.1. states that a purpose of a convolution encoder (paragraph 9.4.1.) is to convey signals through imperfect channels subject to noise and fading. The Office Action has admitted (page 4, lines 3-4) that the Trellis Encoder 32 of Citta is a convolution encoder. Thus, the Trellis Encoder 32 of Citta

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[7] MPEP, §1243.01.

handles noise and fading. As such, the asserted motivation on page 4, lines 11-12 of the Office Action appears to be limited to (i) "minimizing" channel noise and fading and (ii) making the operation of the proposed combination "more efficient and reliable". However, no evidence has been provided that the turbo encoder 502 of Yi would (i) minimize channel noise and fading or (ii) improve efficiency and reliability. In particular, column 12, lines 16-17 of Yi indicate that the Turbo Encoder 502 will "combat" channel noise and fading. However, nothing in Yi appears to indicate that the Turbo Encoder 502 can "minimize" channel noise and fading. Therefore, the asserted "minimize" motivation appears to be merely a conclusory statement. Furthermore, the Office Action has not provided evidence that the Turbo Encoder 502 of Yi would make the system of Citta more efficient and reliable. Therefore, the asserted "more efficient and reliable" motivation also appears to be merely a conclusory statement. Thus, *prima facie* obviousness has not been established to combine the references. Claim 6 provides language similar to claim 1. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 11 provides a converter configured to convert a symbol stream comprising a plurality of symbols into a stream having an encoding and a turbo decoder configured to decode the stream to produce a data stream without the encoding. Page 5, last

paragraph of the Office Action asserts that a Postcoder 48 from FIG. 2A of Citta is similar to the claimed converter. The Office Action also asserts (page 6, lines 11-17) that it would have been obvious to replace the Viterbi Decoder 46 from FIG. 2A of Citta with a turbo decoder. However, the Office Action has failed to provide any evidence that the Postcoder 48 of Citta has a reasonable expectation of operating successfully if positioned upstream of the decoder 46. In particular, column 7, lines 10-13 of Citta state that the Postcoder 48 recovers estimations of input bits X1 and X2 from the decoder 46. Nothing in Citta appears to indicate that the Postcoder 48 can convert a symbol stream into an stream having an encoding that is removed by the decoder 46 (Viterbi or Turbo). The Office Action appears to be moving blocks around in FIG. 2A of Citta without regard for the corresponding functionality of the blocks while using the claims as a template. Therefore, *prima facie* obviousness has not been established for lack of evidence for a reasonable expectation of success.

Claim 11 further provides a turbo decoder configured to decode a stream to produce a data stream. However, the Office Action has failed to establish *prima facie* obviousness to modify Citta to add a Turbo decoder. As argued above for claim 1, the motivation to "minimize" and "make more efficient" appear to be merely conclusory statements. No evidence has been provided in the Office Action why replacing the Viterbi Decoder 46 of Citta with a

Turbo decoder would result in the asserted improvements. As such, *prima facie* obviousness to modify Citta has not been established.

Claim 11 further provides a synchronization remover configured to remove a synchronization signal from a data stream. In contrast, Office Action admits (page 6, lines 1-2) that Citta does not teach or suggest a synchronization remover. However, the Office Action has failed to provide clear and particular evidence for motivation to add a synchronization remover to Citta. Instead, the Office Action merely concludes (page 6, lines 9-10) that adding a synchronization remover would make the system "more efficient". No explanation has been provided why the Symbol Deinterleaver 52, Byte Deinterleaver 54 or the Reed Solomon Decoder 56 of Citta would somehow operate more efficiently if a new circuit were added. As such, *prima facie* obviousness has not been established to modify Citta to include a synchronization remover as presently claimed.

Furthermore, the absence of all but one claimed element in Citta highly suggests that the Office Action was using claim 11 as a template to modify Citta. The Office Action has failed to provide particular findings as to the reasons why a skilled artisan, with no knowledge of the presently claimed invention, would have selected the cited modifications to Citta. The factual inquiry whether to modify the reference must be thorough and searching. The rigorous application of the requirement for showing the teaching or motivation to modify is necessary to avoid the

subtle but powerful attraction of a hindsight-based obviousness analysis. It is improper, in determining whether a person of ordinary skill in the art would have been led to the modification simply to use that which the inventor taught against its teacher. As such, because the Office Action fails to provide particular findings as to the reasons a skilled artisan, with no knowledge of the presently claimed invention, would have selected the cited modifications, the Office Action does not appear to have met the Office's burden of factually establishing a *prima facie* case of obviousness (MPEP §2142). Claim 16 provides language similar to claim 11. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 2 contains all of the limitations of claim 1. Therefore, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 2.

Claim 2 further provides that the transport stream defines two high definition television programs substantially simultaneously. In contrast, Citta and Yi both appear to be silent regarding two high definition television programs in any signal substantially simultaneously. Furthermore, Applicants respectfully traverse the assertion on page 4, lines 14-17 of the Office Action that multiple HDTV programs are implied by broadcast transport streams. In particular, the third paragraph on the first page of

Appendix B states, "The digital broadcasting standards enable transmission of HDTV and multiple SDTV programs with the same channel." While broadcast transport streams may carry multiple standard definition TV programs simultaneously, high definition programs appear to be limited to one at a time. Claims 7, 12 and 17 provide for language similar to claim 2. Therefore, the Examiner is respectfully requested to either (i) provide evidence that transport streams can carry multiple HDTV programs simultaneously or (ii) withdrawn the rejection for claims 2, 7, 12 and 17.

Claim 13 contains all of the limitations of claim 11. Therefore, the arguments presented above in support of the patentability of claim 11 are incorporated hereunder in support of claim 13.

Claim 13 further provides a plurality of decode modules configured to decode a stream to produce a data stream. In contrast, page 7 of the Office Action states "see rejection of claim 11(c)." However, the rejection of claim 11(c) fails to mention a plurality of decode modules. Therefore, Citta, Yi and Official Notice, alone or in combination, do not appear to teach or suggest a plurality of decode modules configured to decode a stream to produce a data stream as presently claimed. As such, claim 13 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 21 contains all of the limitations of claim 1. Therefore, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 21.

Claim 21 further provides a bit-to-symbol mapper configured to map an encoded stream to produce a symbol stream carrying a plurality of symbols each consisting of two error protected bits and one redundant bit. The Office Action (page 7, last paragraph) has asserted that the Mapper and Sync Inserter 34 from FIG. 2A of Citta is similar to the claimed bit-to-symbol mapper. However, the Office Action has also asserted that the same Mapper and Sync Inserter 34 is similar to the claimed formatter and the claimed inserter as noted earlier. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest at least two elements of a formatter, an inserter and a bit-to-symbol mapper as presently claimed. As such, claim 21 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 22 contains all of the limitations of claim 1. Therefore, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 22.

Claim 22 further provides a turbo encoder having a bit error rate not greater than 2 errors per 10,000 bits. The Office Action (page 8) states "See rejection of claim 1(d)." However, the

reasoning for rejecting claim 1(d) is silent regarding a bit error rate. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest a turbo encoder having a bit error rate not greater than 2 errors per 10,000 bits as presently claimed. As such, claim 22 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 23 contains all of the limitations of claim 11. Therefore, the arguments presented above in support of the patentability of claim 11 are incorporated hereunder in support of claim 23.

Claim 23 further provides a demodulator configured to demodulate a signal to produce a symbol stream wherein each of the symbols consists of two error protected bits and one redundant bit. In contrast, Citta and Yi each appear to be silent regarding a demodulated signal of symbols where each symbol consists of two error protection bits and one redundant bit. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest a demodulator configured to demodulate a signal to produce a symbol stream wherein each of the symbols consists of two error protected bits and one redundant bit as presently claimed. As such, claim 23 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 24 contains all of the limitations of claim 16. Therefore, the arguments presented above in support of the

patentability of claim 16 are incorporated hereunder in support of claim 24.

Claim 24 further provides a bit error rate not greater than 3 errors per 100,000 bits for decoding. In contrast, both Citta and Yi appear to be silent regarding bit error rates. Furthermore, the Office Action appears to have cited the language from claim 22 in the rejection of claim 24. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest a bit error rate not greater than 3 errors per 100,000 bits for decoding as presently claimed. As such, claim 24 is fully patentable over the cited reference and the rejection should be withdrawn.

COMPLETENESS OF THE OFFICE ACTION

Aside from a notice of allowance, Applicants' representative respectfully requests any further action on the merits be presented as a non-final action. 37 CFR §1.104(b) states:

> (b) *Completeness of examiner's action.* The examiner's **action will be complete as to all matters**, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

in contrast, no arguments were made in the Office Action to claims 13, 22 and 24. Furthermore, MPEP §707.07(f) reads:

> Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and **answer the substance** of it. (Emphasis added)

Applicants traversed the assertion in the April 24, 2003 Office Action that there was evidence of motivation to combine Citta with Yi (page 13, last paragraph of the July 22, 2003 Amendment). However, the October 22, 2003 Office Action repeated the same motivation language and only added "see rejection of claims 1, 11 and 16" (page 10, Examiner's Response, line "a" of the Office Action). Therefore, the October 22, 2003 Office Action failed to answer the substance of the traverse. As such, the October 20, 2003 Office Action is incomplete.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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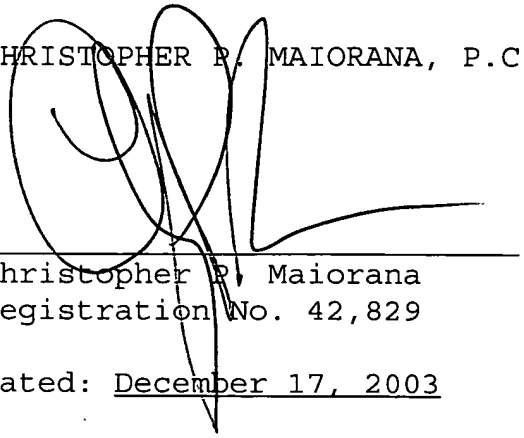

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